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L28: Entry 1 of 1 File: DWPI Mar 14, 2000

DERWENT-ACC-NO: 2000-285798
DERWENT-WEEK: 200025

TITLE: Interconnection structure formation method for multilayer wiring board, involves embedding copper in wiring groove after ashing process by oxygen gas plasma to remove resist film

PRIORITY-DATA: 1998JP-0241887 (August 27, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2000077410 A	March 14, 2000		013	H01L021/3205

INT-CL (IPC): H01L 21/3065; H01L 21/316; H01L 21/3205; H01L 21/768

ABSTRACTED-PUB-NO: JP2000077410A
BASIC-ABSTRACT:

NOVELTY - The wiring groove is formed by etching the silica film with dielectric constant of 3.5 using resist film as mask of conductive material which is embedded in the wiring groove. The resist film is removed by executing ashing process by oxygen gas plasma by maintaining pressure of 1.2 Torr in ashing apparatus.

USE - For formation of multilayer wiring board.

ADVANTAGE - Maintains low dielectric constant by avoiding binding of silicon and hydrogen. Reduces pore Zond generation by using organic SOG.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of formation of multilayer interconnection structure.

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AN 97:81390 USPATFULL

TI Electronic device with a spin-on glass dielectric layer

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PI US 5665845 19970909 <--

AI US 1996-609589 19960301 (8)

RLI Division of Ser. No. US 1994-214477, filed on 17 Mar 1994, now patented, Pat. No. US 5527872 which is a continuation-in-part of Ser. No. US 1990-582570, filed on 14 Sep 1990, now patented, Pat. No. US 5302198

DT Utility

FS Granted

EXNAM Primary Examiner: Marquis, Melvyn I.

LREP Gunter, Jr., Charles D., Bailey, Wayne P.

CLMN Number of Claims: 8

ECL Exemplary Claim: 1

DRWN 1 Drawing Figure(s); 1 Drawing Page(s)

LN.CNT 787

PI US 5665845 19970909 <--

AB There is provided electronic devices with dielectric layers obtained from boron-**oxide** doped, spin-on glass formulations which form glassy layers with high oxygen resistance. Suitable electronic devices include integrated circuits. With high oxygen resistance, the glassy layer formed maintains its integrity in subsequent processing. Also provided is a method for preparing boron-**oxide** doped, spin-on glass formulations with a high carbon content having a silane adhesion promoter and boron-dopant incorporated therein.

SUMM . . . an etch back process wherein after deposition, the spin-on glass layer is etched back to partially expose an underlying CVD **oxide**. The spin-on glass material remains in the voids providing a planarized surface. Another CVD **oxide** is then deposited over this planarized surface. The spin-on glass which remains only fills surface voids in this procedure and does not function as a continuous dielectric layer in the electronic device. The CVD **oxide** provides the continuous dielectric interlayer for the electronic device. In non-etchback processes, the spin-on glass layer is left in place. . . . and helps serve to isolate multilayer metallizations. These continuous spin-on glass layers typically are encapsulated between two layers of CVD **oxide** to isolate the spin-on glass since it is vulnerable to attack (etching) in subsequent processing such as etching baths and. . . . et al., U.S. Pat. No. 4,885,262, describes a method wherein the spin-on glass layer is encapsulated by an underlying CVD **oxide** and a modified surface obtained by treating the spin-on glass layer with siliating agents followed by oxygen annealing.

SUMM . . . oxygen concentration. A typical etching process uses a plasma such as a mixture of CHF.sub.3 and O.sub.2. When the underlying **oxide** is exposed, it releases additional oxygen into the plasma, causing a significant increase in the etch rate of the spin-on. . . . to severe attack causing the film to shrink and crack. Where a spin-on glass dielectric layer is encapsulated with CVD **oxide** layers, it is still exposed to the oxygen plasma in the via cut. The spin-on glass exposed within the via. . . .

SUMM . . . are achieved by this invention through the use and manufacture of an organo-silicon based spin-on glass formulation which contains a boron-**oxide** dopant. This formulation provides spin-on glass layers with improved resistance to ashing by oxygen plasma which can function as a. . . . electronic device. The dielectric interlayer can be a "stand alone" dielectric layer or a dielectric interlayer

encapsulated with two CVD **oxide** layers.

SUMM The process for producing a boron-**oxide** doped, spin-on glass composition provided by this invention comprises dissolving a polyorganosiloxane polymer in an inert organic solvent, adding boric. . .

DETD . . . to printed circuit boards. The electronic devices of this invention have a dielectric layer, preferably an interlayer, comprised of a boron-**oxide** doped glassy layer, derived from a polyorganosiloxane spin-on glass formulation containing boron-**oxide**. The amount of boron-**oxide** within the spin-on glass formulation can vary widely and is preferably greater than 1 wt. % based on the total weight of the formulation. Most preferably, the spin-on glass formulation contains between 2 and 5 wt. % of the boron-**oxide** dopant, based on the total weight of the formulation; however, amounts as high as 30 wt. % of the boron-**oxide** dopant will provide suitable results.

DETD . . . "stand alone" spin-on glass dielectric layers, particularly for high density/large scale integrated circuits, such as VLSI or ULSI circuits. These boron-**oxide** doped spin-on-glass layers can be capped with layers of silicon dioxide, oxynitride, nitride, a spin-on silanating layer or another spin-on-glass. . . or polysiloxane) In high density/large scale integrated circuits, it is preferable to cap or encapsulate the spin-on glass layer with **oxide** films to further protect against degradation from subsequent processing. For example, the dielectric interlayers can be encapsulated between plasma enhanced PE-CVD-ILD **oxide** layers having a thickness of from about 500 .ANG.-10,000 .ANG.. An alternative to applying a capping layer is to form an **SiO**.sub.2 layer from the boron-**oxide** doped spin-on-glass layer. This can be accomplished by a number of conventional techniques such as using a short RIE oxygen. . . by applying another layer such as hexamethyldisiloxane to react with the spin-on-glass to strip away carbon and form a thin **SiO**.sub.2 film. The latter method is performed in a furnace or RTP system.

DETD . . . the wafer is etched (F, Br or CI plasma) followed by removal of the resist. The dielectric interlayers provided by boron-**oxide** doped polyorganosiloxane spin-on glass formulations can provide suitable interconnects through vias deeper than 1 micron, with aspect ratios ranging from. . .

DETD The boron-**oxide** doped, spin-on glass formulation used to produce the dielectric interlayer is based on a polyorganosiloxane polymer. **Spin**-on **glass** formulations based on polyorganosiloxane polymers having a high **organic** content provide thick films without cracking during cure. However, the carbon present is susceptible to reaction with oxygen, forming carbon. . .

DETD The spin-on glass formulations used to provide the dielectric interlayer in the electronic devices of the present invention have a boron-**oxide** dopant incorporated therein. Not wishing to be bound by theory, it is believed the boron-**oxide** dopant incorporates into the organopolysiloxane polymer to form a solution of a metallosiloxane dopant polymer. The boron-**oxide** content of the spin-on glass formulation can vary widely and is preferably greater than 1 wt. %, most preferably from 2 to 5 wt. %; however, much higher levels such as 30 wt. % boron **oxide** are effective. The boron-**oxide** dopant can be introduced into the formulation with a reactive boron compound such as a free acid of boric **oxide**. Preferred compounds contain both boron and oxygen. Trimethylborate and alkoxides or **oxides** of boric acid which are soluble in an inert organic solvent are also suitable. The reactive boron compound is preferably. . . example of such a reactive compound while trimethylborate has shown limited success with polymethylphenylsiloxane polymers. Alternative methods for providing a boron-**oxide** doped polymer can be used, including producing a siloxane polymer

(resin) with boron-**oxide** molecules incorporated into the polymer framework. The molecular weight of such polymers are at the low end of the 500-200,000. . .

DETD . . . preferably above 80.degree. C. A preferred solvent is N-butanol. This solvent allows higher temperatures to be used in incorporating the boron-**oxide** dopant. These higher temperatures provide for more crosslinking, resulting in a denser spin-on glass layer.

DETD . . . acidic pH may be provided by an organic acid, hydrogen peroxide or by the boric acid used to provide the boron-**oxide** dopant. The viscosity of the spin-on glass composition preferably ranges from about 3.5 to 9 centistokes at the preferred solvent. . .

DETD The boron-**oxide** doped spin-on glass compositions utilized to form the dielectric interlayer within the electronic device of this invention is prepared by. . .

DETD . . . at least until the boric acid dissolves, typically about 1-12 hours, more typically about 4 hours for preferred levels of boron-**oxide** dopant. Long reflux times can be used to build up the molecular weight and provide thicker films. The solvent to. . .

DETD . . . that forms during reaction. The dielectric interlayers within the electronic devices of the present invention can be produced from the boron-**oxide** doped, spin-on glass formulations by conventional spin coat techniques wherein a substrate such as a semiconductor is spun at a rate in excess of 1,000 rpm to generate the uniform layer of the boron-**oxide** doped, spin-on glass formulation. The thickness of the layer can be modified by varying the viscosity of the spin-on glass formulation. The boron-**oxide** doped, spin-on glass formulation is then dried by heating the wafer to about 200.degree. C. Layers in excess of 5,000. . . a temperature of from about 350.degree. to 500.degree. C. to cure the dried spin-on glass and form a smooth uniform, boron-**oxide** doped, silicon-based layer. This layer will function as a dielectric interlayer.

DETD The boron-**oxide** doped, spin-on glass formulation will exhibit low shrinkage once dried. Vertical shrinkage as high as 11% may be acceptable; however, it is preferable for shrinkage to be below about 10%. These boron-**oxide** doped, spin-on glass compositions can provide uniform **oxide** layers in excess of 5,000 .ANG., without cracking or loss in subsequent processing. These layers are sufficiently resistant to oxygen. . .

DETD The boron-**oxide** doped, spin-on glass formulations can be applied to semiconductor substrates, glass substrates, insulator (**oxide**) substrates and metal substrates by methods including the spin method, roller coater method, dipping and pull-up method, spray method, screen. . .

DETD . . . to determine the ashing rate of various spin-on glass materials. The following spin-on glass formulations were evaluated: GR653 (methylpolysiloxane), GR653 (boron-**oxide** doped methylpolysiloxane), GR654 (methylpolysiloxane), GR654 (boron-**oxide** doped methylpolysiloxane), GR710 (methylphenylpolysiloxane) and GR720 (methylphenylpolysiloxane). The GR710 and GR720 formulations contain polyorganosiloxane polymers with a silane adhesion promoter. . .

DETD Boron-**Oxide** Doped, Spin-on Glass Formulation

DETD The following process is suitable to incorporate the boron-**oxide** dopant into a polyorganosiloxane polymer. The polyorganosiloxane resin is mixed with either propylene glycol monomethylether (PM), propyleneglycolmonomethylether acetate (PMA) or. . .

DETD . . . theory, it is believed that the oxygen radical in the plasma reacts with the boron to form a B.sub.2 O.sub.3 **oxide** crust Or B.sub.2 O.sub.3 crystals which fill the pores in the polymer network which inhibits further diffusion of the oxygen. . .

DETD . . . undoped, methylpolysiloxane, spin-on glass formulations

exhibited cracks after each ashing experiment. The majority of the layers obtained from the GR653 boron-**oxide** doped, spin-on glass formulations did not crack except for the sample ashed for 5 minutes. Layers from the GR654 boron-**oxide** doped, spin-on glass formulation did not crack until the ashing time exceeded 2 minutes. These films may have cracked prematurely. . .

DETD The GR653 boron-**oxide** doped, spin-on glass formulation provided layers with a higher ashing resistance than layers from the GR653 undoped, spin-on glass formulation. The boron-**oxide** is incorporated into the base polymer by a refluxing operation which also densities the base polymer. The carbon is not totally removed from those layers prepared from the GR653 boron-**oxide** doped, spin-on glass formulations until the ashing time exceeds 15 minutes. The maximum film shrinkage was again 35%, which indicates. . . operation did not lower the carbon content of the film. The majority of the spin-on glass layers from the GR653 boron-**oxide** doped formulations did not crack after the ashing tests except for the 5 minute test.

DETD The spin-on glass layers from the GR654 boron-**oxide** doped, spin-on glass formulation exhibited the highest ashing resistance of all spin-on glass layers tested. The film shrinkage after 15. . .

DETD The same procedure used to form the GR653 boron-**oxide** doped formulation was used to produce the GR654 boron-**oxide** doped formulation. There was a difference in the refluxing temperatures (80.degree. C. for GR653 and 90.degree. for GR654), and the. . . (ethanol for GR653, N-butanol for GR654). In addition, after the refluxing procedure was completed, the film thickness for the GR653 boron-**oxide** doped, spin-on glass formulation was approximately 5,000 .ANG., while the film thickness of the GR654 boron-**oxide** doped, spin-on glass formulation was over 1 micron. Not wishing to be bound by theory, it is believed the increase. . . thickness for the GR654 spin-on glass formulation indicates that the condensation rate of the polymer was higher and that more boron-**oxide** may have been incorporated into the polymer.

DETD . . . improvement in the amount of film shrinkage over 15 minute ash in comparison to the methylphenyl-based polyorganosiloxane polymers. The GR654 boron-**oxide** doped, methyl-based, polysiloxane polymer showed a 150% improvement in film shrinkage after 15 minute ash. The incorporation of the boron-**oxide** into the methyl based polyorganosiloxane polymers also improved their cracking resistance of the polymer.

CLM What is claimed is:

1. An electronic device having a dielectric layer, comprised of a boron-**oxide** substituted polyorganosiloxane polymer having greater than 1 wt. % boron-**oxide**, at least 30 atomic wt. % carbon and a silane adhesion promoter incorporated therein.

2. An electronic device as in claim 1, wherein the dielectric layer is an interlayer derived from a boron-**oxide** substituted polyorganosiloxane polymer formulation containing between 2 and 5 wt. % boron-**oxide**, based on the total weight of the formulation.

4. An electronic device as in claim 3, wherein said dielectric interlayer is encapsulated by two **oxide** layers.

. . . An electronic device as in claim 1, wherein the dielectric layer is encapsulated by a plasma enhanced chemically vapor deposited **oxide** under-layer and a silicon dioxide capping layer.

7. An electronic device having a dielectric interlayer comprised of a boron-**oxide** substituted polyorganosiloxane polymer having at least 2 wt. % boron-**oxide** and at least 15 atomic wt. % carbon, having a thickness of from 0.1 to 10 microns and having a. . .

8. An electronic device as in claim 7, wherein the boron-**oxide**

substituted polyorganosiloxane used to form the dielectric interlayer is boron-**oxide** substituted polymethylsiloxane having a weight average molecular weight of from 500-200,000.

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